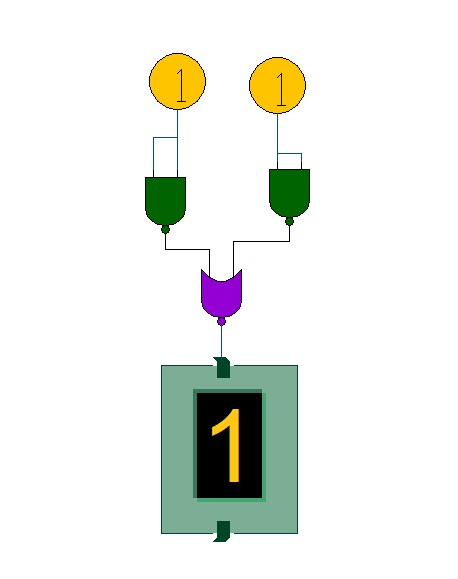
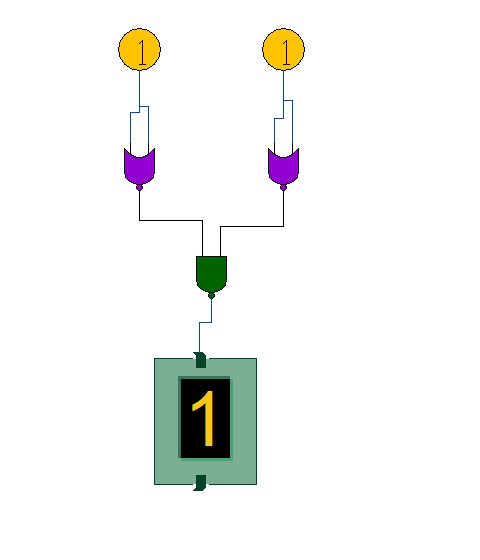
**Q.1 Design AND, OR, and NOT gate using NAND and NOR gate.**

* **AND GATE USING NAND AND NOR GATE**



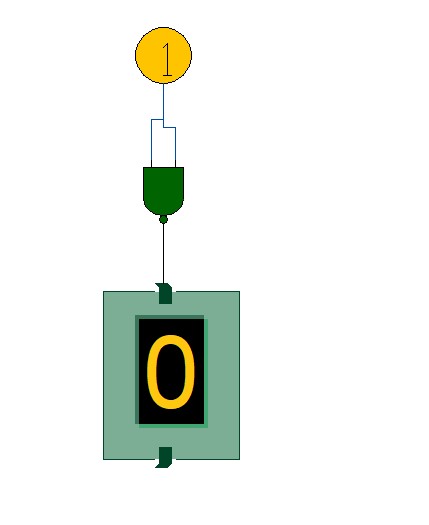
|  |  |  |
| --- | --- | --- |
| **INPUTS** | | **OUTPUT** |
| **A** | **B** | **AB** |
| **0** | **0** | **0** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **1** |

* **OR GATE USING NAND AND NOR GATE.**



|  |  |  |
| --- | --- | --- |
| **INPUTS** | | **OUTPUT** |
| **A** | **B** | **A+B** |
| **0** | **0** | **0** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **1** |

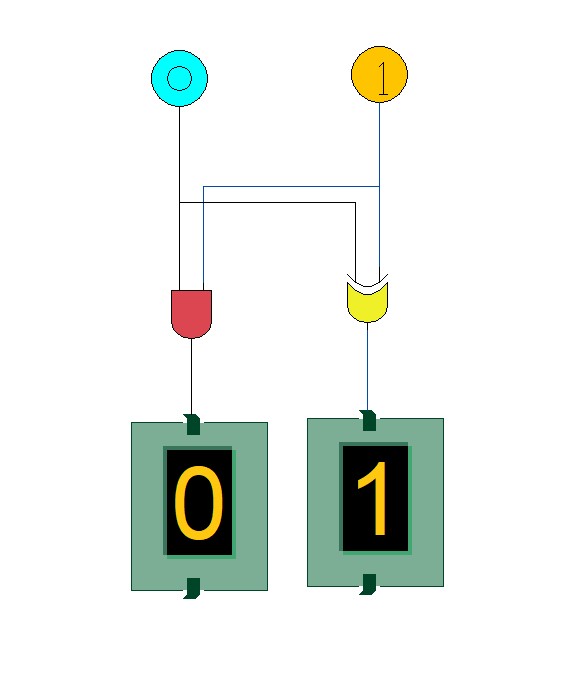
* **OR GATE USING NAND AND NOR GATE .**



|  |  |
| --- | --- |
| **INPUTS** | **OUTPUT** |
| **A** | **B** |
| **0** | **1** |
| **1** | **0** |

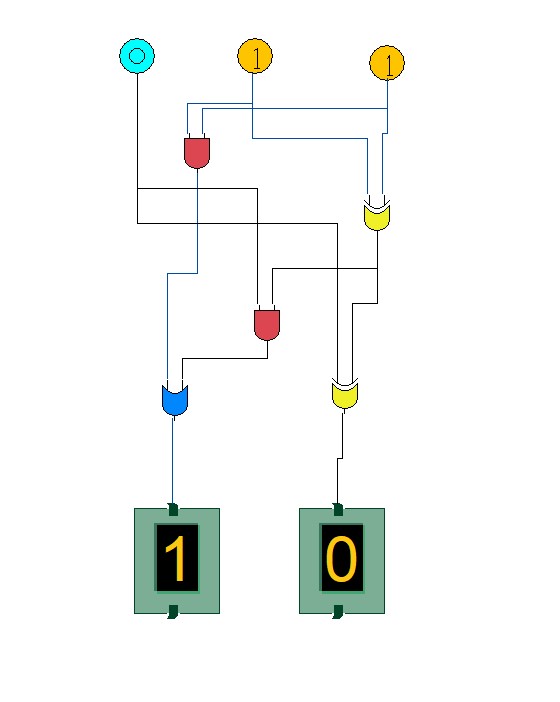
**Q.2 Design a Half Adder and Full adder using basic gates.**

* **Half Adder using Basic gates.**

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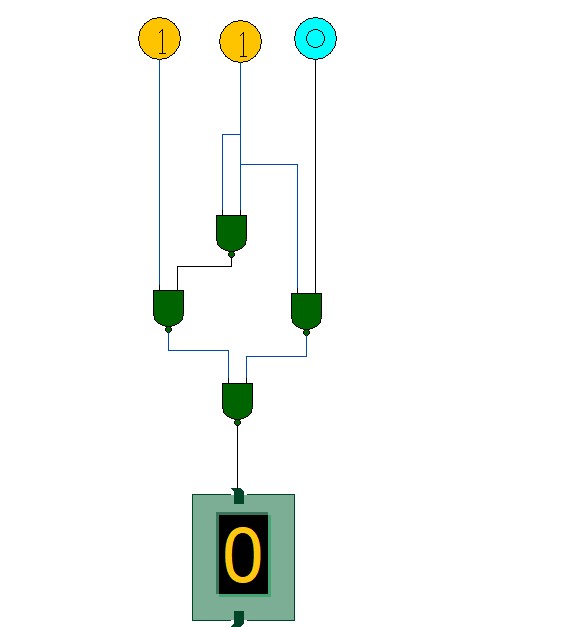
|  |  |  |  |
| --- | --- | --- | --- |
| **INPUT** | | **OUTPUT** | |
| **A** | **B** | **SUM** | **CARRY** |
| **0** | **0** | **0** | **0** |
| **0** | **1** | **1** | **0** |
| **1** | **0** | **1** | **0** |
| **1** | **1** | **0** | **1** |

* **FULL ADDER USING BASIC GATES.**

****

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **INPUTS** | | | **OUTPUT** | |
| **A** | **B** | **Cin** | **SUM** | **CARRY** |
| **0** | **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **1** | **0** |
| **0** | **1** | **0** | **1** | **0** |
| **0** | **1** | **1** | **0** | **1** |
| **1** | **0** | **0** | **1** | **0** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **0** | **0** | **1** |
| **1** | **1** | **1** | **1** | **1** |

**Q.3 To Design and set up 2:1 Multiplexer(MUX) using only NAND gates.**

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|  |  |  |  |
| --- | --- | --- | --- |
| **SELECT LINE** | **INPUTS** | | **OUTPUT** |
| **S** | **A** | **B** | **Y** |
| **0** | **0** | **0** | **0** |
| **0** | **0** | **1** | **0** |
| **0** | **1** | **0** | **1** |
| **0** | **1** | **1** | **1** |
| **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **1** |
| **1** | **1** | **0** | **0** |
| **1** | **1** | **1** | **1** |