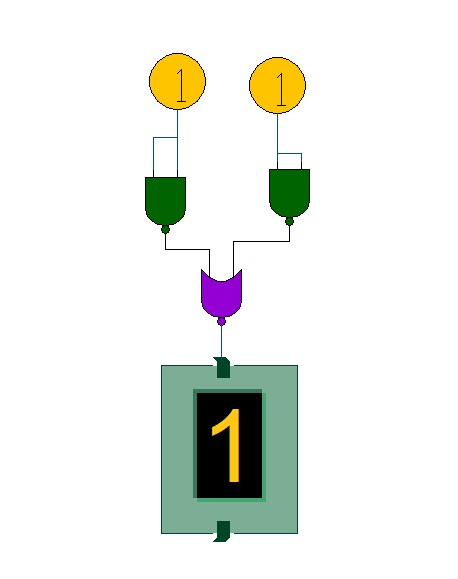
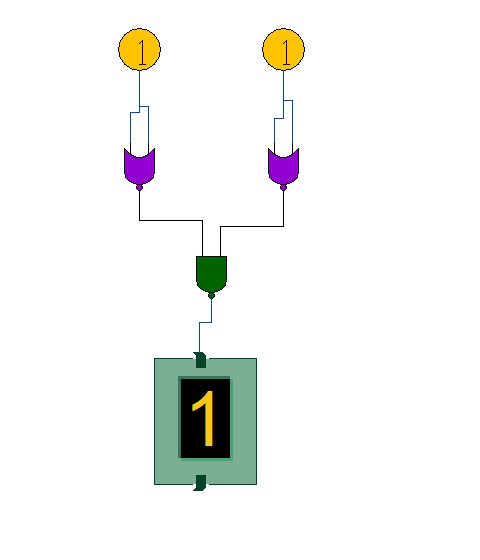
**Q.1 Design AND, OR, and NOT gate using NAND and NOR gate.**

* **AND GATE USING NAND AND NOR GATE**



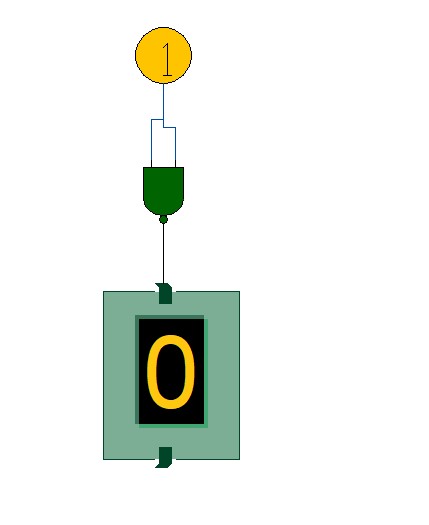
| **INPUTS** | | **OUTPUT** |
| --- | --- | --- |
| **A** | **B** | **AB** |
| **0** | **0** | **0** |
| **0** | **1** | **0** |
| **1** | **0** | **0** |
| **1** | **1** | **1** |

* **OR GATE USING NAND AND NOR GATE**



| **INPUTS** | | **OUTPUT** |
| --- | --- | --- |
| **A** | **B** | **A+B** |
| **0** | **0** | **0** |
| **0** | **1** | **1** |
| **1** | **0** | **1** |
| **1** | **1** | **1** |

* **OR GATE USING NAND AND NOR GATE .**



| **INPUTS** | **OUTPUT** |
| --- | --- |
| **A** | **B** |
| **0** | **1** |
| **1** | **0** |

